THE FOLLOWING ARE THE ENGLISH TRANSLATION OF ANNEXES TO THE INTERNATIONAL PRELIMINARY EXAMINATION REPORT (ARTICLE 34):

Amended Sheets (Pages 21-25)

English translation of the amended sheets of International Preliminary Examination Report

CLAIMS

1. Sealing processing for two wafers (2, 12) made of semiconducting materials, comprising:

- a step for implantation of metallic species (4) in at least the first wafer, through an assembly surface with the second wafer,
- a step for assembly of the first and second wafer by molecular bonding,
- a step for formation of metallic compounds, forming a pure resistive metallic contact between the two wafers at the assembly interface of these wafers, alloys between the implanted metallic species and the semiconducting materials of the two wafers.

2. Process according to claim 1, the formation step of the metallic compounds resulting from a heat treatment at a temperature equal at least to the formation temperature of the said compounds.

3. Process according to claim 1 or 2, the metallic species being implanted at a depth (Rp) of between 5 nm and 20 nm under the surface (6) of the implanted wafer.

4. Process according to one of claims 1 to 3, the metallic species being implanted at a dose of between 10^{14} and a few 10^{18} species/cm^2.

5. Process according to one of claims 1 to 4, also comprising an amorphisation step before assembly to make all or part of the surface layer of the first wafer amorphous.

6. Process according to claim 5, the amorphisation step comprising deposition of an amorphous material layer before and/or after implantation of metallic species.

7. Process according to claim 5, the amorphisation step comprising a surface implantation, for example by hydrogen or metallic species.

8. Process according to one of claims 1 to 7, each of the wafers being made from a material chosen from among silicon, gallium arsenide (GaAs), SiC (silicon carbide), InP (Indium phosphide), Germanium (Ge), le silicon - Germanium (SiGe).

9. Process according to one of claims 1 to 8, the implanted species being Nickel and/or palladium and/or Cobalt, and/or Platinum, and/or Tantalum, and/or Tungsten, and/or Titanium, and/or Copper.

10. Process according to one of claims 1 to 9, at least one of the wafers (12) being a heterostructure, for example of the SOI type.

11. Process according to one of claims 1 to 10, at least one of the wafers being thinned, after

assembly or after the formation step of metallic compounds.

12. Process according to one of claims 1 to 11, at least one of the wafers being a debondable structure.

13. Process according to one of claims 1 to 12, at least one of the wafers comprising a weakening plane.

14. Process according to claim 13, the wafer comprising a weakening plane being thinned by fracture along the said weakening plane, after assembly or after the formation step of the metallic compounds.

15. Process according to one of claims 1 to 14, at least one of the wafers comprising at least one circuit or circuits layer, on or close to its face to be assembled.

16. Process according to one of claims 1 to 15, the implantation step of metallic species being done through a mask (30) to obtain local implantation zones (32, 34).

17. Process according to one of claims 1 to 15, also comprising the formation of an insulating layer (20) on the first wafer, before it is implanted with metallic species.

English translation of the amended sheets of International Preliminary Examination Report

18. Process according to one of claims 1 to 17, also comprising a thinning step of the implanted wafer after implantation of metallic species.

19. Process according to one of claims 1 to 18, the first wafer comprising at least one insulating zone (48, 50) located at the surface so as to obtain local implantation zones (54).

20. Structure composed of two substrates made of semiconducting materials assembled by molecular bonding obtained using a process according to one of claims 1 to 19, and having localised zones (42, 44, 54, 56, 64) of metallic compounds at the assembly interface, these metallic compounds being alloys made from semiconducting materials of substrates at the assembly interface and at least one metal chosen from among nickel, palladium, cobalt, platinum, tantalum, tungsten, titanium, copper.

21. Structure according to claim 20, the semiconducting materials being chosen from among Si, GaAs, SiC, InP, SiGe.

22. Structure according to claim 20 or 21, at least one of the substrates being a heterostructure.

23. Structure according to one of claims 20 to 22, at least one of the substrates being a thin film.

English translation of the amended sheets of International Preliminary Examination Report

24. Structure according to one of claims 20 to 23, at least one of the substrates comprising electronic and/or optical and/or mechanical components.

25. Structure according to one of claims 20 to 24, one of the substrates being a thin film (41) made of silicon comprising RF circuits (43, 45).

26. Structure according to claim 25, the other substrate (40) being made of high resistivity silicon.